

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2397	SERIAL NO. 10/671,228
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Shubneesh Bhatnagar et al.	
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U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
<i>Lee</i>	AA	5,728,621	03/98	Zheng et al.			
	AB	5,834,358	11/98	Pan et al.			
	AC	5,923,993	07/99	Sahota			
	AD	5,817,567	10/98	Jang et al.			
	AE	5,387,539	02/95	Yang et al.			
	AF	5,915,190	06/99	Pirkle			
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	AH	5,665,202	09/97	Subramanian et al.			
	AI	5,459,096	10/95	Venkatesan et al.			
	AJ	5,904,539	05/99	Hause et al.			
<i>Lee</i>	AK	5,872,045	02/99	Lou et al.			

FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
AL							
AM							
AN							
AO							
AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)		
AR		S. Wolf, Silicon Processing for the VLSI Era, Volume 2 - Process Integration (Published by Lattice Press, Copyright 1990) (pgs. 229-232)
AS		
AT		

EXAMINER <i>Kevin Ming Lee</i>	DATE CONSIDERED 3/30/04
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U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
<i>Lee</i>	AA	5,435,888	07/95	Kalnisky et al.				
	AB	6,274,498	08/01	Moore et al.				
	AC	4,656,497	04/87	Rogers et al.				
	AD	5,735,333	04/98	Gilmore et al.				
	AE	5,920,792	07/99	Lin				
<i>Lee</i>	AF	4,769,340	09/88	Chang et al.				
	AG	5,759,913	06/98	Fulford, Jr. et al.				
	AH							
	AI							
	AJ							
	AK							
FOREIGN PATENT DOCUMENTS								
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